IN THE CLAIMS

Claims 22-44 are now pending. Please amend the claims as follows (all pending claims are reproduced for the Examiner's convenience):

Please cancel claims 1-21.

Please add new claims 22-44:

22. (New) A semiconductor memory device including a plurality of transistors, wherein each of the transistors comprises:

a semiconductor layer of a first conduction type and electrically isolated from other memory cells such that it is floating;

a drain diffusion region of a second conduction type, formed in the first conduction-type semiconductor layer, and connected to a bit line;

a source diffusion region of the second conduction type, formed apart from the drain diffusion region in the first conduction-type semiconductor layer, and connected to a source line; and

a gate electrode formed on the semiconductor layer between the drain diffusion region and the source diffusion region with a gate insulator therebetween, and forms a word line,

wherein the transistor has a first data state having a first threshold voltage in which excessive majority carriers are held in the semiconductor layer and a second data state having a second threshold voltage in which the excessive majority carriers in the semiconductor layer are emitted,

and wherein the bit line is one of a plurality of bit lines, a sense amplifier being provided

for the plurality of bit lines, one of the bit lines being selected to be connected to the sense amplifier.

23. (New) The semiconductor memory device according to claim 22,

wherein the first data state is a state in which impact ionization is generated near a drain junction by operating the transistor and in which excessive majority carriers produced by this impact ionization are held in the semiconductor layer, and

the second data state is a state in which a forward bias is applied between the semiconductor layer and the drain diffusion region to extract the excessive majority carriers from within the semiconductor layer to the drain diffusion region.

24. (New) The semiconductor memory device according to claim 22, wherein the semiconductor layer is a silicon layer formed on a silicon substrate with an insulating film therebetween.

25. (New) The semiconductor memory device according to claim 24, wherein the silicon layer is a p-type, and the transistor is an N-channel MOS transistor.

26. (New) The semiconductor memory device according to claim 22, wherein a voltage of the source line is constant.

27. (New) The semiconductor memory device according to claim 26, wherein when data is written, with the source line as a reference voltage,

a first voltage higher than the reference voltage is given to a word line of a selected transistor,

a second voltage lower than the reference voltage is given to a word line of a non-

selected transistor,

a third voltage higher than the reference voltage is given to the bit line when the first data state is written,

and a fourth voltage lower than the reference voltage is given to the bit line when the second data state is written.

28. (New) The semiconductor memory device according to claim 27, wherein when the data is read,

with the source line as the reference voltage,

a fifth voltage, which is between the first threshold voltage and the second threshold voltage and higher than the reference voltage, is given to the word line of the selected transistor to detect whether the selected transistor conducts.

29. (New) The semiconductor memory device according to claim 27, wherein when the data is read, with the source line as the reference voltage,

a fifth voltage, which is higher than the first and second threshold voltages and higher than the reference voltage, is given to the word line of the selected transistor to detect a conductivity of the selected transistor.

30. (New) The semiconductor memory device according to claim 27, wherein when the data is read, after the voltage of the word line is raised more than the second threshold voltage, a predetermined current is supplied to the bit line to detect a potential difference in the bit line.

31. (New) The semiconductor memory device according to claim 27, wherein when the data is read, after the voltage of the word line is raised more than the second threshold voltage, a

current is supplied to the bit line to clamp the voltage thereof at a predetermined voltage and to detect a difference in the supplied current.

32. (New) A semiconductor memory device, comprising:

an SOI substrate in which a silicon layer is formed on an insulating film formed on a silicon substrate;

a plurality of transistors which have drain diffusion regions and source diffusion regions formed in the silicon layer and gate electrodes formed on the silicon layer, wherein pairs of the transistors, each pair sharing one of the drain diffusion regions, being arranged in a matrix form and element-isolated in a channel width direction, wherein the gate electrodes of the transistors arranged in a first direction are continuously formed so as to form word lines; and

a plurality of bit lines running in a second direction intersecting the first direction and connected to the drain diffusion regions of the transistors;

wherein each of the transistors has a first data state having a first threshold voltage in which excessive majority carriers are held in the silicon layer and a second data state having a second threshold voltage in which the excessive majority carriers in the silicon layer are emitted,

wherein a sense amplifier is provided for the plurality of bit lines, one of the bit lines being selected to be connected to the sense amplifier.

33. (New) The semiconductor memory device according to claim 32, wherein the transistors, each having a cell size of $2F \times 2F$ where F is a minimum feature size, are arranged in a matrix form.

34. (New) The semiconductor memory device according to claim 32, wherein the drain

diffusion region and the source diffusion region are formed sufficiently deep to reach the insulating film located under the silicon layer.

35. (New) The semiconductor memory device according to claim 32,

wherein the first data state is a state in which impact ionization is generated near a drain junction by operating the transistor and in which excessive majority carriers produced by this impact ionization are held in the silicon layer, and

the second data state is a state in which a forward bias is applied between the silicon layer and the drain diffusion region to extract the excessive majority carriers from within the silicon layer to the drain diffusion region.

36. (New) The semiconductor memory device according to claim 32, wherein the silicon layer is a p-type, and the transistor is an N-channel MOS transistor.

37. (New) The semiconductor memory device according to claim 32, wherein a voltage of the source diffusion regions is constant.

38. (New) The semiconductor memory device according to claim 37, wherein when data is written, with the source diffusion regions as a reference voltage,

a first voltage higher than the reference voltage is given to a word line of the selected transistor,

a second voltage lower than the reference voltage is given to a word line of the non-selected transistor,

a third voltage higher than the reference voltage is given to the bit line when the first data state is written,

and a fourth voltage lower than the reference voltage is given to the bit line when the second data state is written.

39. (New) The semiconductor memory device according to claim 38, wherein when the data is read, with the source diffusion regions as the reference voltage,

a fifth voltage, which is between the first threshold voltage and the second threshold voltage and higher than the reference voltage, is given to the word line of the selected transistor to detect whether the selected transistor conducts.

40. (New) The semiconductor memory device according to claim 38, wherein when the data is read, with the source diffusion regions as the reference voltage,

a fifth voltage, which is higher than the first and second threshold voltages and higher than the reference voltage, is given to the word line of the selected transistor to detect a conductivity of the selected transistor.

41. (New) The semiconductor memory device according to claim 32, wherein when the data is read, after a voltage of a word line of the selected transistor is raised more than the second threshold voltage, a predetermined current is supplied to a bit line of the selected transistor to detect a potential difference in the bit line thereof.

42. (New) The semiconductor memory device according to claim 32, wherein when the data is read, after a voltage of a word line of the selected transistor is raised more than the second threshold voltage, a current is supplied to a bit line of the selected transistor to clamp the voltage thereof at a predetermined voltage and to detect a difference in the supplied current.

43. (New) The semiconductor memory device according to claim 38, wherein when the

data is read, after a voltage of a word line of the selected transistor is raised more than the second threshold voltage, a predetermined current is supplied to a bit line of the selected transistor to detect a potential difference in the bit line thereof.

44. (New) The semiconductor memory device according to claim 38, wherein when the data is read, after a voltage of a word line of the selected transistor is raised more than the second threshold voltage, a current is supplied to a bit line of the selected transistor to clamp the voltage thereof at a predetermined voltage and to detect a difference in the supplied current.